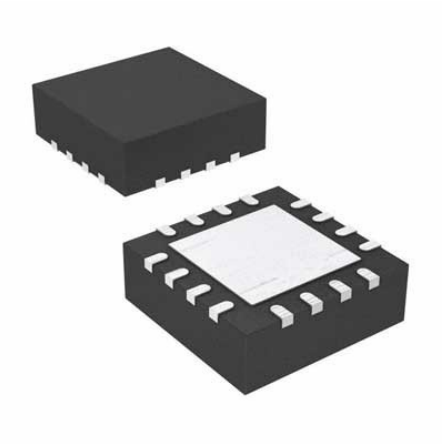
SY89872UMG

Data Sheet

2.5V, 2GHz ANY DIFF. IN-TO-LVDS PROGRAMMABLE CLOCK DIVIDER/FANOUT BUFFER WITH INTERNAL TERMINATION

Manufacturers	Microchip Technology, Inc
Package/Case	VQFN-16
Product Type	Clock & Timer ICs
RoHS	Rohs
Lifecycle	



Images are for reference only

Please submit RFQ for SY89872UMG or Email to us: sales@ovaga.com We will contact you in 12 hours. RFQ

General Description

This 2.5V low-skew, low-jitter, precision LVDS output clock divider accepts any high-speed differential clock input (AC or DC-coupled) CML, LVPECL, HSTL or LVDS and divides down the frequency using a programmable divider ratio to create a frequency-locked, lower speed version of the input clock. The SY89872U includes two output banks. Bank A is an exact copy of the input clock (pass through) with matched propagation delay to Bank B, the divided output bank.Available divider ratios are 2, 4, 8 and 16. In a typical 622MHz clock system this would provide availability of 311MHz, 155MHz, 77MHz or 38MHz auxiliary clock components.The differential input buffer has a unique internal termination design that allows access to the termination network through a VT pin. This feature allows the device to easily interface to different logic standards. A VREF- AC reference is included for AC-coupled applications.The SY89872U is part of Micrel's high-speed Precision Edge® timing and distribution family. For 3.3V applications, consider the SY89873L. For applications that require an LVPECL output, consider the SY89872U.The /RESET input asynchronously resets the divider outputs (Bank B). In the pass-through function (Bank A) the /RESET synchronously enables or disables the outputs on the next falling edge of IN (rising edge of /IN). Refer to the "Timing Diagram."

Features

Guaranteed AC performance over temperature and voltage:

Low jitter design

265 RMS phase jitter

Unique input termination and VTpin for DC-coupled and AC-coupled inputs: any differential inputs (LVPECL, LVDS, CML, HSTL)

Precision differential LVDS outputs

Matched delay: all outputs have matched delay, independent of divider setting

TTL/CMOS inputs for select and reset/disable

Two output banks (matched delay)

Bank A: Buffered copy of input clock (undivided)

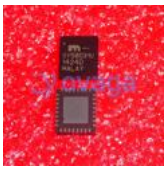
Bank B: Divided output (÷2, ÷4, ÷8, ÷16), two copies

2.5V power supply

Wide operating temperature range: -40°C to +85°C

Available in 16-pin (3mm x 3mm) QFN package

Related Products



SY58031UMG

Microchip Technology, Inc

VQFN-32

SY89467UHY

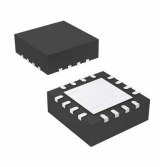
Microchip Technology, Inc

TQFP-64

SY58034UMG

Microchip Technology, Inc

VQFN-32



SY89833LMG

Microchip Technology, Inc

VQFN-16

SY89838UMG

Microchip Technology, Inc

VQFN-32

SY89826LHY

Microchip Technology, Inc

TQFP-64

SY89468UHY

Microchip Technology, Inc

TQFP-64

SY56011RMG

Microchip Technology, Inc

QFN-16