



Data Sheet

1-Channel Single ADC Pipelined 100Msps 16-bit Parallel 100-Pin TQFP EP Tray

Manufacturers Analog Devices, Inc

Package/Case TQFP-100

Product Type Data Conversion ICs

RoHS Rohs

Lifecycle



Images are for reference only

Please submit RFQ for AD9446BSVZ-100 or <u>Emailto:scales@ovaga.com</u> We will contact you in 12 hours.

RFO

General Description

The ADC requires 3.3 V and 5.0 V power supplies and a low voltage differential input clock for full performance operation. No external reference or driver components are required for many applications. Data outputs are LVDS-compatible (ANSI-644) or CMOS-compatible and include the means to reduce the overall current needed for short trace distances.

Optional features allow users to implement various selectable operating conditions, including data format select and output data mode.

The AD9446 is available in a 100-lead surface-mount plastic package (100-lead TQFP/EP) specified over the industrial temperature range (-40° C to $+85^{\circ}$ C).

PRODUCT HIGHLIGHTS

APPLICATIONS

True 16 bit linearity.

High performance: outstanding SNR performance for baseband IFs in data acquisition, instrumentation, magnetic resonance imaging, and radar receivers.

Ease of use: On-chip reference and high input impedance track-and-hold. An output clock simplifies data capture.

Packaged in a Pb-free, 100-lead TQFP/EP.

Clock duty cycle stabilizer (DCS) maintains overall ADC performance over a wide range of clock pulse widths.

OR (out-of-range) outputs indicate when the signal is beyond the selected input range.

Features

100 MSPS guaranteed sampling rate (AD9446-100)

83.6 dBFS SNR with 30 MHz input (3.8 V p-p input, 80 MSPS)

82.6 dBFS SNR with 30 MHz input (3.2 V p-p input, 80 MSPS)

89 dBc SFDR with 30 MHz input (3.2 V p-p input, 80 MSPS)

95 dBFS 2-tone SFDR with 9.8 MHz and 10.8 MHz (100 MSPS)

60 fsec rms jitter

Excellent linearity

2.0 V p-p to 4.0 V p-p differential full-scale input

Buffered analog inputs

LVDS outputs (ANSI-644 compatible) or CMOS outputs

Data format select (offset binary or twos complement)

Output clock available

3.3 V and 5 V supply operation

Related Products



ADAS3022BCPZ
Analog Devices, Inc
LFCSP-40



AD574AJNZ
Analog Devices, Inc
PDIP-28



AD7938BSUZ
Analog Devices, Inc
TQFP-32



AD7124-8BCPZ-RL7
Analog Devices, Inc
LFCSP-32

Application

MRI receivers

Multi-carrier, multimode cellular receivers

Antenna array positioning

Power amplifier linearization

Broadband wireless

Radar, infrared imaging

Communications instrumentation



AD7266BSUZ
Analog Devices, Inc
TQPF-32



AD7401YRWZ

Analog Devices, Inc
SOIC-16



AD7192BRUZ-REEL
Analog Devices, Inc
TSSOP-24



AD9680BCPZ-500

Analog Devices, Inc

LFCSP-64