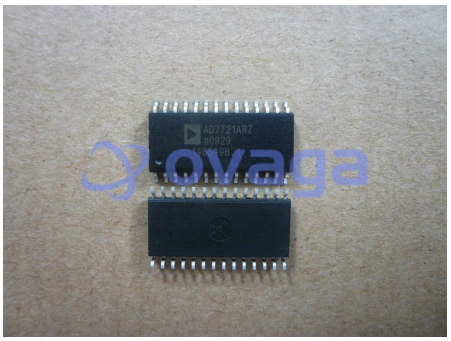
AD7721ARZ

Data Sheet

CMOS, 12-/16-Bit, 312.5 kHz/468.75 kHz Sigma-Delta ADC; Package: SOIC - Wide; No of Pins: 28; Temperature Range: Industrial

Manufacturers	Analog Devices, Inc
Package/Case	SOIC-28
Product Type	Data Conversion ICs
RoHS	Rohs
Lifecycle	



Images are for reference only

Please submit RFQ for AD7721ARZ or Email to us: sales@ovaga.com We will contact you in 12 hours. RFQ

General Description

The AD7721 is a complete low power, 12-/16-bit, sigma-delta ADC. The part operates from a +5 V supply and accepts a differential input of 0 V to 2.5 V or ±1.25 V. The analog input is continuously sampled by an analog modulator at twice the clock frequency eliminating the need for external sample-and-hold circuitry. The modulator output is processed by two finite impulse response (FIR) digital filters in series. The on-chip filtering reduces the external antialias requirements to first order in most cases. Settling time for a step input is 218.4 µs while the group delay for the filter is 109.2 µs when the master clock equals 15 MHz.

The AD7721 can be operated with input bandwidths up to 229.2 kHz. The corresponding output word rate is 468.75 kHz. The part can be operated with lower clock frequencies also. The sample rate, filter corner frequency, settling time, group delay and output word rate will be reduced also, as these are proportional to the external clock frequency. The maximum clock frequencies in parallel mode and serial mode are 10 MHz and 15 MHz respectively.

Use of a single bit DAC in the modulator guarantees excellent linearity and dc accuracy. Endpoint accuracy is ensured by on-chip calibration of offset and gain. This calibration procedure minimizes the part's zero-scale and full-scale errors.

The output data is accessed from the output register through a serial or parallel port. This offers easy, high speed interfacing to modern microcontrollers and digital signal processors. The serial interface operates in internal clocking (master) mode, the AD7721 providing the serial clock.

CMOS construction ensures low power dissipation while a power-down mode reduces the power consumption to only 100 µW.

Features

16-Bit Sigma-Delta ADC

468.75 kHz Output Word Rate (OWR)

No Missing Codes

Low-Pass Digital Filter

High Speed Serial Interface

Linear Phase

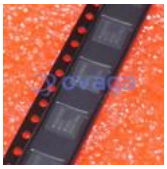
229.2 kHz Input Bandwidth

Power Supplies: AVDD, DVDD: +5 V ± 5%

Standby Mode (70 µW)

Parallel Mode (12-Bit/312.5 kHz OWR)

Related Products



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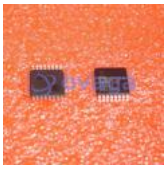
Analog Devices, Inc

LFCSP-40



[AD7266BSUZ]

Analog Devices, Inc

TQPF-32

[AD574AJNZ]

Analog Devices, Inc

PDIP-28

[AD7401YRWZ]

Analog Devices, Inc

SOIC-16

[AD7938BSUZ]

Analog Devices, Inc

TQFP-32

[AD7192BRUZ-REEL]

Analog Devices, Inc

TSSOP-24

[AD7124-8BCPZ-RL7]

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LFCSP-32

[AD9680BCPZ-500]

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LFCSP-64