

2:4 LVDS 1.8V / 2.5V Fanout Buffer for 1PPS and High-Speed Clocks

Manufacturers

[Renesas Technology Corp](#)

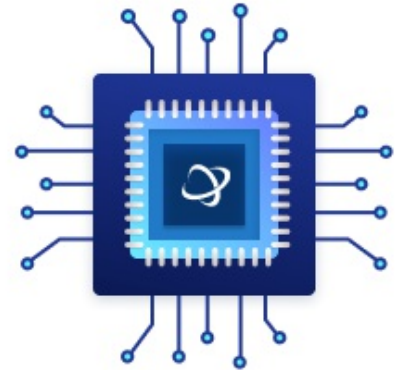
Package/Case

Product Type

Clock & Timer ICs

RoHS

Lifecycle



Images are for reference only

Please submit RFQ for 8P34S1204NLGI8 or [Email to us: sales@ovaga.com](mailto:sales@ovaga.com) We will contact you in 12 hours.

[RFQ](#)

General Description

The 8P34S1204 is a high-performance differential LVDS fanout buffer. The device is designed for the fanout of 1PPS signals or high-frequency, very low additive phase-noise clock and data signals. The 8P34S1204 supports fail-safe operation and is characterized to operate from a 1.8V or 2.5V power supply. Guaranteed output-to-output and part-to-part skew characteristics make the 8P34S1204 ideal for those clock distribution applications demanding well-defined performance and repeatability. Two selectable differential inputs and four low skew outputs are available. The integrated bias voltage reference enables easy interfacing of single-ended signals to the differential device input. The device is optimized for low power consumption and low additive phase noise.

Features

Four low skew, low additive jitter LVDS output pairs

Two selectable, differential clock input pair

Differential CLK, nCLK pairs can accept the following differential input levels: LVDS, CML

Maximum input clock frequency: 1.5GHz

Output skew: 10ps (typical)

Propagation delay: 400ps (maximum)

Low additive phase jitter, RMS;>

Device current consumption (IDD):

65mA typical: 1.8V

75mA typical: 2.5V

Full 1.8V or 2.5V supply voltage

Lead-free (RoHS 6), 16-Lead VFQFN package

Supports case temperature up to +105°C

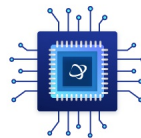
Supports PCI Express Gen 1-5

Related Products



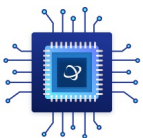
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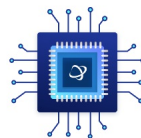
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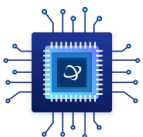
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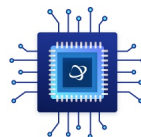
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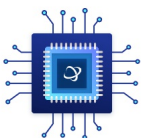
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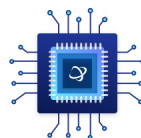
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