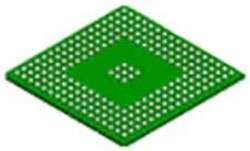
ADSP-21262SBBCZ150

Data Sheet

Digital Signal Processors & Controllers - DSP, DSC 150 MHz 32Bit DSP Processor.

Manufacturers	Analog Devices, Inc
Package/Case	CSPBGA-136
Product Type	Digital Signal Processors & Controllers - DSP, DSC
RoHS	Rohs
Lifecycle	



Images are for reference only

Please submit RFQ for ADSP-21262SBBCZ150 or Email to us: sales@ovaga.com We will contact you in 12 hours. RFQ

General Description

The ADSP-21262 is the first member of the third-generation of SHARC® programmable DSPs. A range of applications such as high-quality audio and automotive entertainment systems, voice recognition, medical appliances and measurement devices benefit from the ADSP-21262's integration of large on-chip memory with a wide variety of peripherals—thereby speeding time to market and keeping costs low.

The ADSP-21262 is based on the SHARC DSP core that supports execution of 32-bit fixed-point and 32/40-bit floating-point arithmetic formats.With its core running at 200MHz (5 ns instruction cycle time), the ADSP-21262 is capable of executing complex Fast Fourier Transform (FFT) operations—1024-point complex FFT in 46us, more than 2.6x faster than comparatively priced processors.In audio applications, the single-instruction, multiple data (SIMD) mode effectively doubles the processor performance.

The ADSP-21262 is designed with the highest level of integration, including 2 Mbit of on-chip dual-ported SRAM and 4 Mbit of mask programmable ROM memory.This large on-chip dual-ported memory enables sustained processor and I/O performance, without the need for external memory.System I/O is achieved through six full-duplex serial ports, four timers, a 16-bit parallel port, a serial peripheral interface (SPI), 22 zero-overhead Direct Memory Access (DMA) channels delivering fast data transfers without processor intervention and an innovative Digital Applications Interface (DAI) offering complete software control through its Signal Routing Unit (SRU).

Digital Applications Interface (DAI) for Simplified I/O System DevelopmentThe ADSP-21262 introduces the Digital Applications Interface (DAI), an architecture that enables complete software programmability of various peripherals.The flexibility and ease-of-use of the SHARC programming model, combined with the DAI, allow manufacturers to deploy one hardware configuration into multiple product offerings with different I/O requirements.

Connections are made using the flexible Signal Routing Unit (SRU), a matrix routing group of pins that provides configurable and flexible connectivity between all DAI components and the SRU.The peripherals connected through the DAI are: a precision clock generator (PCG), an input data port (IDP), six SPORTS (serial ports), six flag inputs, six flag outputs, three timers and the SRU.The IDP provides an additional input path to the DSP core, configurable as 8 channels of receive serial data or as 7 channels of receive serial data and a single channel of up to a 20-bit wide parallel data.This level of integration enables the designer to take full advantage of a wide variety of peripherals without sacrificing the overall system performance.

CROSSCORE Development Tools 3rd Generation SHARC DSP members are supported by ADI's CROSSCORE brand of award winning development tools. The CROSSCORE components include the VisualDSP++™ software development environment, EZ-KIT Lite™ evaluation systems, and emulators.

VisualDSP++ is an integrated software development environment, allowing for fast and easy development, debug, and deployment. The EZ-KIT Lite evaluation system provides an easy way to investigate the power of the ADI family of DSPs and begin to develop applications. Emulators are available for PCI and USB host platforms for rapid on-chip debugging. Additional development tools and algorithms are available from an extensive third-party development community.

Features

200MHz (5ns) SIMD SHARC Core, capable of 1.2GFLOPS

Code compatible with all SHARC DSPs

Supports IEEE-compatible 32-bit floating-point, 40-bit floating-point and 32-bit fixed-point data types

2Mbit on-chip dual-ported SRAM; 4Mbit mask-programmable ROM

2.4Gbyte/sec on-chip bandwidth

6 independent Serial Ports - Supports: Standard DSP Serial mode, I2S mode, Left Justified Sample pair mode and TDM mode

22 Zero-overhead DMA channels

SPI compatible interface and a 16-bit Parallel Port

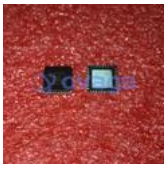
Digital Applications Interface (DAI)

PLL capable of a variety of software multiplier ratios

Four timers: 1 core and 3 general purpose timers supporting PWM generation mode, PWM capture/pulse width measurement mode and external event watchdog mode

136-ball BGA (12mm x 12mm) and 144-lead LQFP (20mm x 20mm) packages available in Commercial and Industrial temp ranges

Related Products



ADUC7022BCPZ62

Analog Devices, Inc

LFCSP-40

ADUC7020BCPZ62

Analog Devices, Inc

LFCSP-40

ADUC841BSZ62-5

Analog Devices, Inc

QFP-52

ADUC841BSZ62-3

Analog Devices, Inc

QFP-52

ADUC831BSZ

Analog Devices, Inc

QFP-52

ADSP-BF527BBCZ-5A

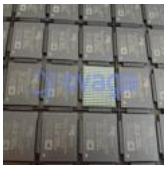
Analog Devices, Inc

BGA-208

[ADSP-21369BBPZ-2A]

Analog Devices, Inc

SBGA-256



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Analog Devices, Inc

CSPBGA-256