



Data Sheet

10-Bit, 210 MSPS ADC; Package: TQFP-EP (14x14mm w/9.5mm EP); No of Pins: 80; Temperature Range: Industrial

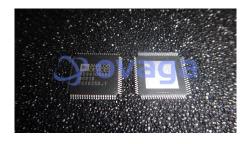
Manufacturers <u>Analog Devices, Inc</u>

Package/Case TQFP-80

Product Type Data Conversion ICs

RoHS Rohs

Lifecycle



Images are for reference only

Please submit RFQ for AD9410BSVZ or Emailto:sales@ovaga.com We will contact you in 12 hours.

RFO

General Description

The AD9410 is a 10-bit monolithic sampling analog-to-digital converter (ADC) with an on-chip track-and-hold circuit and is optimized for high speed conversion and ease of use. The product operates at a 210 MSPS conversion rate, with outstanding dynamic performance over its full operating range.

The ADC requires a 5.0 V and 3.3 V power supply and up to a 210 MHz differential clock input for full performance operation. No external reference or driver components are required for many applications. The digital outputs are TTL-/CMOS-compatible and separate output power supply pins also support interfacing with 3.3 V logic.

The clock input is differential and TTL-/CMOS-compatible. The 10-bit digital outputs can be operated from 3.3 V (2.5 V to 3.6 V) supplies. Two output buses support demultiplexed data up to 105 MSPS rates and binary or twos complement output coding format is available. A data sync function is provided for timing-dependent applications. An output clock simplifies interfacing to external logic. The output data bus timing is selectable for parallel or interleaved mode, allowing for flexibility in latching output data.

Fabricated on an advanced BiCMOS process, the AD9410 is available in an 80-lead thin quad flat package, exposed pad specified over the industrial temperature range (-40° C to $+85^{\circ}$ C).

Product Highlights

High Resolution at High Speed—The architecture is spe-cifically designed to support conversion up to 210 MSPS with outstanding dynamic performance.

Demultiplexed Output—Output data is decimated by two and provided on two data ports for ease of data transport.

Output Data Clock—The AD9410 provides an output data clock synchronous with the output data, simplifying the timing between data and other logic.

Data Synchronization—A DS input is provided to allow for synchronization of two or more AD9410s in a system, or to synchronize data to a specific output port in a single AD9410 system.

Features

500 MHz analog bandwidth

On-chip reference and track and hold

1.5 V p-p differential analog input range

5.0 V and 3.3 V supply operation

3.3 V CMOS/TTL outputs

Power: 2.1 W typical at 210 MSPS

Demultiplexed outputs each at 105 MSPS

Output data format option

Data sync input and data clock output provided

Interleaved or parallel data output option

Application

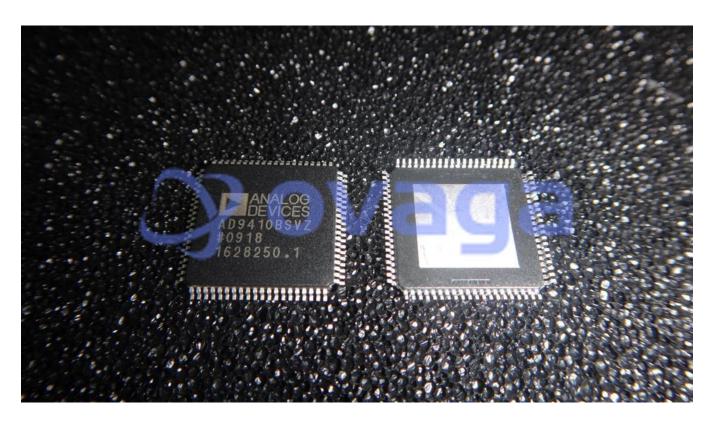
Communications and radars

Local multipoint distribution services (LMDS)

High-end imaging systems and projectors

Cable reverse paths

Point-to-point radio links



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